# 2014-04

**mardi 08/04**

**on wafer QPSLN1,  mask CPBv1+NbSi carac**
- spin S1813 4000rpm
- bake 1' @ 115°C (set)
- expo 15" @ 9.2mW/cm2
- dev 2'30 in MF 319

OK

**lundi 14/04**

**Etch RIE**: try to put less voltage to induce less defect in Si
CF4 30cc / Ar 15cc, P=210µb, 30W -> 90V

It seems that the layer etches away already without plasma, as the interference patterns moves when I introduce the gas!
I was not properly aligned with the laser, so I waited too long (5'10) which yielded a 140nm step

**Second litho**
- spin AZ5214E 4000rpm
- bake 1' @ 110°C (set)
- vac expo 3" @ 9.2mW/cm2
- bake 2'30 @ 125°C (set)
- flood expo 25" @ 9.2mW/cm2
- dev 1' in MIF 726

OK

NB: I had to mask half of the wafer to expose only the NbSi carac patterns (but not the CPB patterns).
For the first step (S1813) I masked with aluminum foil on top of the mask
For the second step (AZ5214) I exposed the whole wafer 3", then masked the NbSi patterns on the wafer with an Al foil and exposed them 3" again. So these patterns were exposed 3" or 6". In the end, I could see a differential in the development rate of 3" and 6" layers, inducing a step of 70nm (out of 1770nm).

**Evap**
- 150nm Al @ 2nm/s

**Lift** aceton, easy.

**Spin** S18 to protect from cutting
Diamond scriber, easy, all 6 chips recovered

**lundi 28/04**

First chip to measure: field-effect
Bonding parameters are difficult to find.